IN THE CLAIMS

1. (Currently Amended) A semiconductor device, comprising:

a plurality of metal line patterns having a predetermined surface area size, wherein two adjacent metal line patterns are spaced a predetermined distance less than 10 μm apart from each other [at a predetermined distance].

2. (Original) A semiconductor device as claimed in claim 1, wherein the predetermined distance is greater than 1.0 μm.

3. (Original) A semiconductor device as claimed in claim 1, wherein the predetermined distance is greater than 1.5 μm.

4. (Original) A semiconductor device as claimed in claim 1, wherein the plurality of metal line patterns have a surface area size of greater than "30μm×30μm".

5. (Currently Amended) A semiconductor device, comprising:

a metal line layer having a plurality of metal line patterns spaced less than 10 μm apart from each other; and

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at least one underlying layer under the metal line layer,

wherein the space between two adjacent metal line patterns has a sufficient width to prevent a crack from occurring in the underlying layer.

6. (Original) A semiconductor device as claimed in claim 5, wherein the width of the space is greater than 1.0 μm.

7. (Original) A semiconductor device as claimed in claim 5, wherein the width of the space is greater than 1.5 μm.

8. (Original) A semiconductor device as claimed in claim 5, wherein the underlying layer is an insulating layer.

9. (Original) A semiconductor device as claimed in claim 5, wherein the metal line pattern has a surface area size of greater than "30μm×30μm".

10. (Currently Amended) A semiconductor device, comprising:

a plurality of metal line patterns, wherein two adjacent metal line patterns are spaced less than 10 μm apart from each other, and at least one of the two adajacent metal line patterns has a slit.

11. (Original) A semiconductor device as claimed in claim 10, wherein the slit has a width of greater than 1.0 μm.

12. (Original) A semiconductor device as claimed in claim 11, wherein the slit is formed at a predetermined distance from an edge of the metal line pattern.

13. (Original) A semiconductor device as claimed in claim 12, wherein the predetermined distance is less than 4 μm.

14. (Currently Amended) A semiconductor device having a multi-layered structure, comprising:

A' cont'd

a metal line layer having a plurality of metal line patterns spaced less than 10 μm apart from each other;

at least one underlying layer under the metal line layer; and

a slit formed at a sufficient distance from a space between two adjacent metal line patterns to prevent a crack from occurring in the underlying layer.

15. (Original) A semiconductor device as claimed in claim 14, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

16. (Original) A semiconductor device as claimed in claim 14, wherein the slit has a width greater than 1.0 μm.

17. (Original) A semiconductor device as claimed in claim 14, wherein the distance from the space between the two adjacent metal line patterns to the slit is less than 4.0 μm.

18. (Withdrawn) A method of manufacturing a semiconductor device having a multi-layered structure, comprising:

forming at least one underlying layer on a semiconductor substrate; and

forming a metal line layer on the underlying layer, the metal line layer having a plurality of metal line patterns spaced apart from each other at a predetermined distance.

19. (Withdrawn) A method as claimed in claim 18, wherein the predetermined distance is greater than 1.0 μm.

20. (Withdrawn) A method as claimed in claim 18, wherein the predetermined distance is greater than 1.5 μm.

21. (Withdrawn) A method of manufacturing a semiconductor device having a multi-layered structure, comprising:

forming at least one underlying layer on a substrate;

forming simultaneously a metal line layer on the underlying layer and a slit, the metal line layer having a plurality of metal line patterns spaced apart from each other, at least one of either of two adjacent metal lines has a slit.

A' cont'd

22. (Withdrawn) A method as claimed in claim 21, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

23. (Withdrawn) A method as claimed in claim 21, wherein a width of the slit is greater than 1.0 μm.

24. (Withdrawn) A method as claimed in claim 21, wherein a distance from the space between two adjacent metal line patterns to the slit is less than 4.0 μm.

25. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming at least one underlying layer on a substrate;

forming simultaneously a metal line layer on the underlying layer and a slit, the metal line layer having a plurality of metal line patterns spaced apart from each other, the slit formed at a sufficient distance from a space between the two adjacent metal line patterns in order to prevent a crack from occurring in the underlying layer.

26. (Withdrawn) A method as claimed in claim 25, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

27. (Withdrawn) A method as claimed in claim 25, wherein the width of the slit is greater than 1.0 μm.

28. (Withdrawn) A method as claimed in claim 25, wherein the distance between the slit and the space between two adjacent metal line patterns is less than 4.0 μm.

29. (New) A semiconductor device, comprising:

a plurality of metal line patterns, wherein two adjacent metal line patterns are spaced less than 1.5 μm apart from each other, and at least one of the two adajacent metal line patterns has a slit.

30. (New) A semiconductor device having a multi-layered structure, comprising:

a metal line layer having a plurality of metal line patterns spaced apart from each other;

at least one underlying layer under the metal line layer; and

a slit formed less than 4 μm from a space between two adjacent metal line patterns in order to prevent a crack from occurring in the underlying layer.